CHAPTER 5. CIRCUIT DESCRIPTION

[1] Circuit description

1. General description

The compact design of the control PWB is obtained by using CONEXANT fax engine in the main control section and high density printing of surface mounting parts. Each PWB is independent according to its function as shown in Fig. 1.

2. PWB configuration

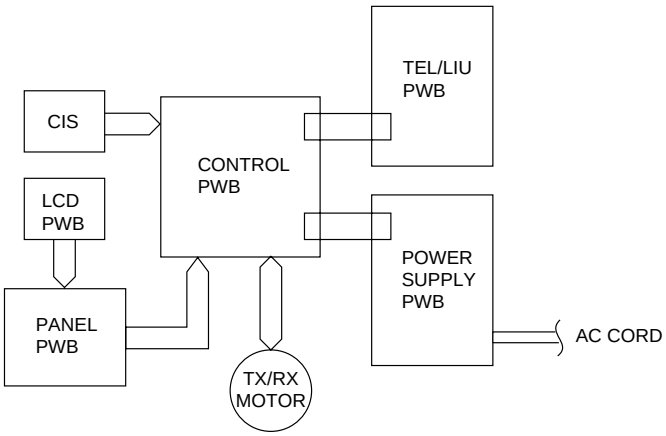


Fig. 1

1) Control PWB

The control PWB controls peripheral PWBs, mechanical parts, transmission, and performs overall control of the unit.
This machine employs a 1 chip modem (FM209) which is installed on the control PWB.

2) TEL/LIU PWB

This PWB controls connection of the telephone line to the unit.

3) Power supply PWB

This PWB provides voltages of +5V and +24V to the other PWBs.

4) Panel PWB

The panel PWB allows input of the operation keys.

5) LCD PWB

This PWB controls the LCD display.

3. Operational description

Operational descriptions are given below:

- Transmission operation

  When a document is loaded in standby mode, the state of the document sensor is sensed via the 1 chip fax engine (FC200). If the sensor signal was on, the motor is started to bring the document into the standby position. With depression of the START key in the off-hook state, transmission takes place.
  Then, the procedure is sent out from the modem and the motor is rotated to move the document down to the scan line. In the scan processor, the signal scanned by the CIS is sent to the internal image processor and the AD converter to convert the analog signal into binary data. This binary data is transferred from the scan processor to the image buffer within the RAM and encoded and stored in the transmit buffer of the RAM. The data is then converted from parallel to serial form by the modem where the serial data is modulated and sent onto the line.

- Receive operation

  There are two ways of starting reception, manual and automatic.
  Depression of the START key in the off-hook mode in the case of manual receive mode, or CI signal detection by the LIU in the automatic receive mode.

  First, the FC200 controls the procedure signals from the modem to be ready to receive data. When the program goes into phase C, the serial data from the modem is converted to parallel form in the modem interface of the 1 chip fax engine (FC200) which is stored in the receive buffer of the RAM. The data in the receive buffer is decoded software-wise to reproduce it as binary image data in the image buffer. The data is DMA transferred to the recording processor within the FC200 which is then converted from parallel to serial form to be sent to the thermal head. The data is printed line by line by the FC200 which is assigned to control the motor rotation and strobe signal.

- Copy operation

  To make a copy on this facsimile, the COPY key is pressed when the machine is in stand-by with a document on the document table and the telephone set is in the on-hook state.

  First, depression of the COPY key advances the document to the scan line. Similar to the transmitting operation, the image signal from the CIS is converted to a binary signal in the DMA mode via the 1 chip fax engine (FC200) which is then sent to the image buffer of the RAM. Next, the data is transferred to the recording processor in the DMA mode to send the image data to the thermal head which is printed line by line. The copying takes place as the operation is repeated.

[2] Circuit description of control PWB

1. General description

Fig. 2 shows the functional blocks of the control PWB, which is composed of 4 blocks.

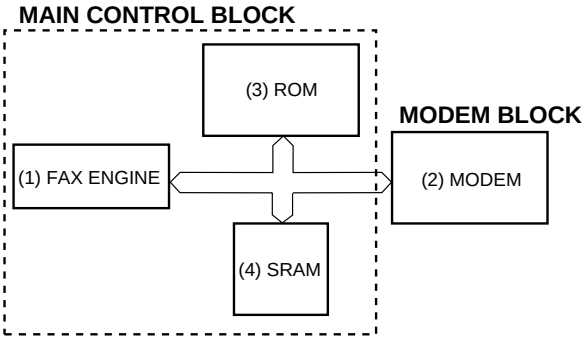


Fig. 2 Control PWB functional block diagram

2. Description of each block

(1) Main control block

The main control block is composed of CONEXANT 1 chip fax engine (FC200), ROM (1Mbit), SRAM (256kbit) and Modem (FM209).
Devices are connected to the bus to control the whole unit.

1) FC200 (IC2) : pin-144 QFP (FAX ENGINE)

2) FM209 (IC4) : pin-128 QFP (MODEM)

The FAX ENGINE Integrated Facsimile Controllers.

FC200, contains an internal 8 bit microprocessor with an external 16 Mbyte address space and dedicated circuitry optimized for facsimile image processing and facsimile machine control and monitoring.

3) 27E010 (IC5): pin-32 DIP (ROM)

ROM of 1 Mbit equipped with software for the main CPU.

4) W24258S-70LE (IC3): pin-28 SOP (SRAM)

Line memory for the main CPU system RAM area and coding/decoding process. Used as the transmission buffer.

Memory of recorded data such as daily report and auto dials. When the power is turned off, this memory is backed up by the lithium battery.

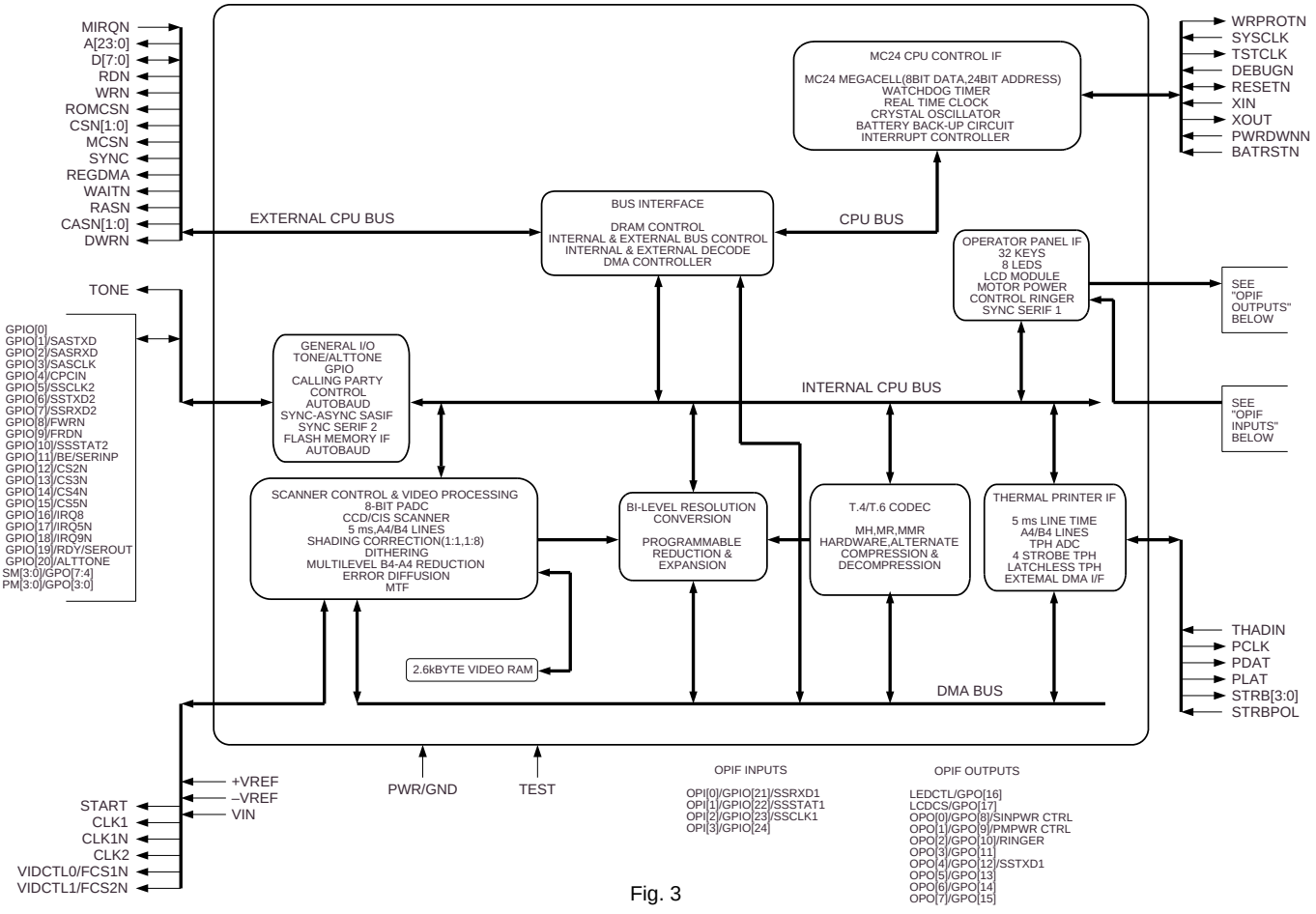


Fig. 3

FC200 (IC2) Terminal descriptions

Pin Name	Pin No.	I/O	Input Type	Output Type	Pin Description (Note: Active low signals have an "n" pin name ending.)
CPU Control Interface					
MIRQn	135	I	HU	–	Modem interrupt, active low. (Hysteresis In, Internal Pullup.)
SYSCLK	133	I	H	–	System clock. (Hysteresis In.)
TSTCLK	130	O	–	123XT	Test clock.
Bus Control Interface					
A[23:0] [15:20][22:27]	[1:6][8:13]	O	TU	123XT	Address bus (24-bit).
D[7:0] [141:144]	[136:139]	I/O	TU	123XT	Data bus (8-bit).
RDn	128	O	–	123XT	Read strobe.
WRn	127	O	–	123XT	Write strobe.
ROMCSn	120	O	–	123XT	ROM chip select.
CS1n	122	O	–	123XT	I/O chip select.
CS0n	57	O	–	123XT	SRAM chip select. (Battery powered.)
MCSn	121	O	–	123XT	Modem chip select.
SYNC	126	O	–	123XT	Indicates CPU op code fetch cycle (active high).
REGDMA	124	O	–	123XT	Indicates REGSEL cycle and DMA cycle.
WAITn	125	O	–	123XT	Indicates current TSTCLK cycle is a wait state or a halt state.
RASn	113	O	–	123XT	DRAM row address select. (Battery powered.)
CAS[1:0]n	[111:112]	O	–	123XT	DRAM column address select. (Battery powered.)
DWRn	109	O	–	123XT	DRAM write. (Battery powered.)
Prime Power Reset Logic and Test					
DEBUGn	129	I	HU	–	External non-maskable input (NMI).
RESETn	131	I/O	HU	2XO	FC100/FC200 Reset.
TEST	58	I	C	–	Sets Test mode (Battery powered).
Battery Power Control and Reset Logic					
XIN	59	I	OSC	–	Crystal oscillator input pin.
XOUT	60	O	–	OSC	Crystal oscillator output pin.
PWRDWNn	62	I	H	–	Used by external system to indicate -to FC200 - loss of prime power. (Results in NMI)
BATRSTn	61	I	H	–	Battery power reset input.
WRPROTn	110	O	–	1XC	(Battery powered.) Write protect during loss of VDD power. NOTE:The functional logic is powered by battery power, but the output drive is powered by DRAM battery power.
Scanner Interface					
START	101	O	–	2XS	Scanner shift gate control.
CLK1	100	O	–	2XS	Scanner clock.
CLK1n	99	O	–	2XS	Scanner clock-inverted.
CLK2	98	O	–	2XS	Scanner reset gate control (or clock for CIS scanner).
FCS1n/VIDCTL0	96	O	–	2XT	Flash memory chip select or Video Control signal.
FCS2n/VIDCTL1	97	O	–	2XT	Flash memory chip select or Video Control signal.
Printer Interface					
PCLK/DMAACK	29	O	–	3XC	Thermal Print Head (TPH) clock, or external DMAACK.
PDAT	30	O	–	2XP	Serial printing data (to TPH).
PLAT	31	O	–	3XP	TPH data latch.
STRB[3:0]	[33:36]	O	–	1XP	Strobe signals for the TPH.
STRBPOL/DMAREQ	37	I	C	–	Sets strobe polarity, active high/low or external DMA request.
Operator Panel Interface					
OPO[0]/GPO[8]/ SMPWRCTRL	47	O	–	2XL	Keyboard/LED strobe [0] or GPO[8] or Scan Motor Power Control
OPO[1]/GPO[9]/ PMPWRCTRL	46	O	–	2XL	Keyboard/LED strobe [1] or GPO[9] or Print Motor Power Control
OPO[2]/GPO[10]/ RINGER	44	O	–	2XCT	Keyboard/LED strobe [2] or GPO[10] or RINGER
OPO[3]/GPO[11]	43	O	–	2XL	Keyboard/LED strobe [3] or GPO[11]
OPO[4]/GPO[12]/ SSTXD1	42	O	–	2XL	Keyboard/LED strobe [4] or GPO[12] or SSTXD1 (for SSIF1)
OPO[5]/GPO[13]	40	O	–	2XL	Keyboard/LED strobe [5] or GPO[13]
OPO[6]/GPO[14]	39	O	–	2XL	Keyboard/LED strobe [6] or GPO[14]
OPO[7]/GPO[15]	38	O	–	2XL	Keyboard/LED strobe [7] or GPO[15]
OPI[0]/GPIO[21]/ SSRXD1	52	I/O	HU	2XC	(Pullup, Hysteresis In) Keyboard return [0] or GPIO[21] or SSRXD1 (for SSIF1)
OPI[1]/GPIO[22]/ SSSTAT1	51	I/O	HU	2XC	(Pullup, Hysteresis In) Keyboard return [1] or GPIO[22] or SSSTAT1 (for SSIF1)

FC200 (IC2) Terminal descriptions

Pin Name	Pin No.	I/O	Input Type	Output Type	Pin Description
Operator Panel Interface					
OPI[2]/GPIO[23]/ SSCLK1	50	I/O	HU	2XC	(Pullup, Hysteresis In) Keyboard return [2] or GPIO[23] or SSCLK1 (for SSIF1)
OPI[3]/GPIO[24]	49	I/O	HU	2XC	(Pullup, Hysteresis In) Keyboard return [3] or GPIO[24]
LEDCTL	55	O	–	4XC	Indicates outputs OPO[7:0] are for LEDs.
LCDCS	54	O	–	1XC	LCD chip select.
General Purpose I/O					
GPIO[0]	94	I/O	H	2XC	(Hysteresis In) GPIO[0].
GPIO[1]/SASTXD	93	I/O	H	2XC	(Hysteresis In) GPIO[1] or SASTXD (for SERIF).
GPIO[2]/SASRXD	92	I/O	H	2XC	(Hysteresis In) GPIO[2] or SASRXD (for SERIF).
GPIO[3]/SASCLK	91	I/O	H	2XC	(Hysteresis In) GPIO[3] or SASCLK (for SERIF).
GPIO[4]/CPCIN	90	I/O	H	2XC	(Hysteresis In) GPIO[4] or Calling Party Control Input.
GPIO[5]/SSCLK2	89	I/O	H	2XC	(Hysteresis In) GPIO[5] or SSCLK2 (for SSIF2).
GPIO[6]/SSTXD2	87	I/O	H	2XC	(Hysteresis In) GPIO[6] or SSTXD2 (for SSIF2).
GPIO[7]/SSRXD2	86	I/O	H	2XC	(Hysteresis In) GPIO[7] or SSRXD2 (for SSIF2).
GPIO[8]/FWRn	85	I/O	H	2XC	(Hysteresis In) GPIO[8] or flash write enable signal for NAND-type flash memory.
GPIO[9]/FRDn	84	I/O	H	2XC	(Hysteresis In) GPIO[9] or flash read enable signal for NAND-type flash memory.
GPIO[10]/SSSTAT2	83	I/O	H	2XC	(Hysteresis In) GPIO[10] or SSSTAT2 (for SSIF2).
GPIO[11]/BE/ SERINP	82	I/O	H	1XC	(Hysteresis In) GPIO[11] or bus enable or serial port data input for autobaud detection.
GPIO[12]/CS[2]n	80	I/O	H	2XC	(Hysteresis In) GPIO[12] or I/O chip select [2].
GPIO[13]/CS[3]n	79	I/O	H	2XC	(Hysteresis In) GPIO[13] or I/O chip select [3].
GPIO[14]/CS[4]n	78	I/O	H	2XC	(Hysteresis In) GPIO[14] or I/O chip select [4].
GPIO[15]/CS[5]n	77	I/O	H	2XC	(Hysteresis In) GPIO[15] or I/O chip select [5].
GPIO[16]/IRQ[8]	76	I/O	H	1XC	(Hysteresis In) GPIO[16] or external interrupt 8.
GPIO[17]	75	I/O	H	1XC	(Hysteresis In) GPIO[17].
GPIO[18]/IRQ[9]n	74	I/O	H	1XC	(Hysteresis In) GPIO[18] or external interrupt 9.
GPIO[19]/RDY/ SEROUT	73	I/O	H	1XC	(Hysteresis In) GPIO[19] or ready signal or Serial port data output for autobaud detection.
GPIO[20]/ALTTONE	107	I/O	H	1XC	(Hysteresis In) GPIO[20] or ALTTONE.
Miscellaneous					
SM[3:0]/GPO[7:4]	[103:106]	O	–	1XC	Programmable: scan motor control pins or GPO pins.
PM[3:0]/GPO[3:0]	[115:118]	O	–	1XC	Programmable: print motor control pins or GPO pins.
TONE	119	O	–	1XC	Tone output signal.
Power, Reference Voltages, Ground					
-Vref/CLREF	66	I	-VR	–	Negative Reference Voltage for Video A/D or Reference Voltage for the Clamp Circuit.
ADXG	68	I	VXG	–	A/D Internal GND. (NOTE: This pin requires an external 0.22µF decoupling capacitor to ADGA.)
ADGA	69		VADG		A/D Analog Ground
ADVA	70		VADV		A/D Analog Power
ADGD	72		VADG		A/D Digital Ground
+Vref	71	I	+VR		Positive Reference Voltage for Video A/D.
VIN	67	I	VA	–	Analog Video A/D input.
THAD1	65	I	TA	–	Analog Thermal A/D input.
Power and Ground					
VSS(12)	7,21,28,45, 53,56,64,88, 95,108,132, 134				Digital Ground
VDD(8)	14,32,41,48, 81,102,123, 140				Digital Power
VBAT	63				Battery Power
VDRAM	114				DRAM Battery Power

(2) Panel control block

The following controls are performed by the FC200.

- Operation panel key scanning
- Operation panel LCD display

(3) Mechanism/recording control block

- Recording control block diagram (1)

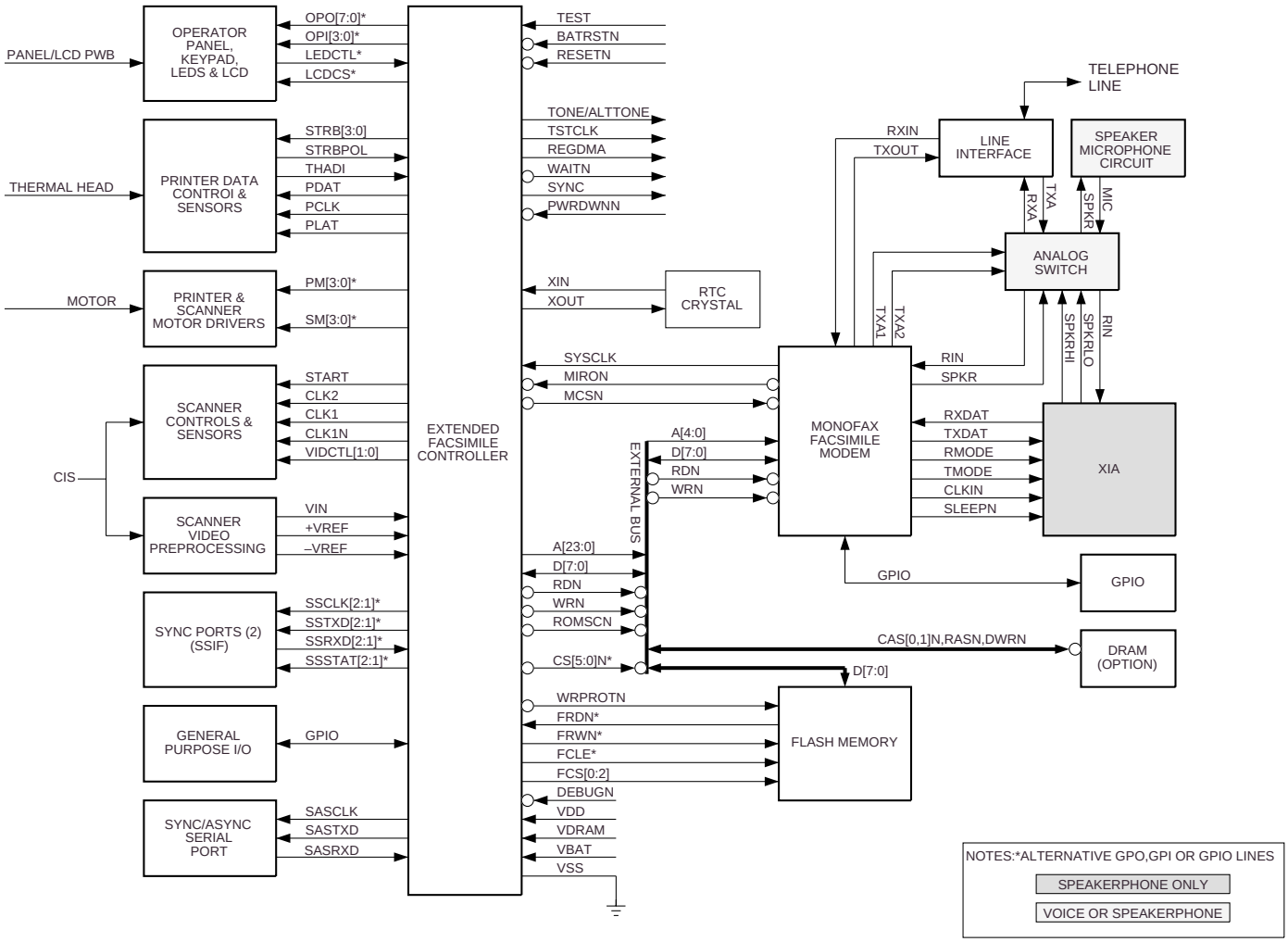


Fig. 4

(4) Modem (FM209) block

INTRODUCTION

The CONEXANT FM209 MONOFAX modem is a synchronous 9600 bits per second (bps) half-duplex modem with error detection and DTMF reception. It has low power consumption and requires a single +5V and +3.3V DC power supply. The modem is housed in a single VLSI device package.
The modem can operate over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA).
The FM209 is designed for use in Group 3 facsimile machines.
The modem satisfies the requirements specified in CCITT recommendations V.29, V.27 ter, V.21 Channel 2 and T.4, and meets the binary signaling requirements of T.30.
The modem can operate at 9600, 7200, 4800, 2400, or 300 bps, and also includes the V.27 ter short training sequence option.
The modem can also perform HDLC framing according to T.30 at 9600, 7200, 4800, 2400, or 300 bps.
The modem features a programmable DTMF receiver and three programmable tone detectors which operate concurrently with the V.21 channel 2 receiver.
The voice mode allows the host computer to efficiently transmit and receive audio signals and messages.
The modem is available in either a 128-pin plastic quad flat pack (TQFP). General purpose input/output (GPIO) pins are available for host as signment in the 128-pin TQFP.
The modem's small size, single voltage supply, and low power consumption allow the design of compact system enclosures for use in both office and home environments.
MONOFAX is a registered trademark of CONEXANT.

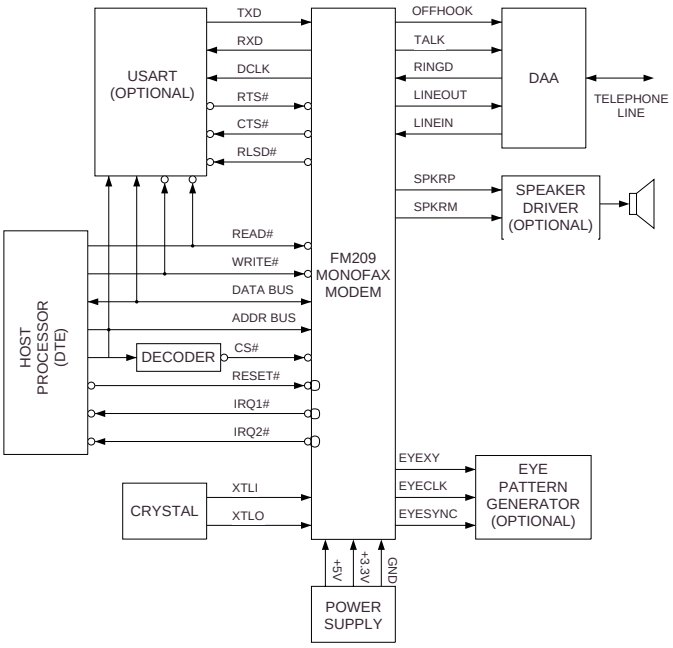


Fig. 5

FEATURES

- Group 3 facsimile transmission/reception
  - ITU-T V.29, V.27 ter, T.30, V.21 Channel 2, T.4
  - ITU-T V.17 and V.27 ter short train
  - HDLC framing at all speeds
  - Receive dynamic range: 0 dBm to -43 dBm
  - Automatic adaptive equalization
  - Fixed and programmable digital compromise equalization
  - DTMF detect and tone detect
  - ITU-T V.21 Channel 2 FSK 7E Flag Detect
  - Ring detector
  - Programmable transmits level
  - Programmable single/dual tone transmission
- V.23 and Type I Caller ID
  - Full-duplex modes:
    TX = 75 bps. RX = 1200 bps
    TX = 1200 bps. RX = 75 bps
  - Half-duplex mode:
    TX = RX = 1200 bps
  - Serial and parallel data modes
  - Programmable parallel data mode
  - 5, 6, 7 or 8 data bits
  - 1 or 2 Stop bits
  - Mark, Space, Even, or Odd Parity
  - Break function
  - Transmitter squelch
  - Compromise equalizer
- Programmable interface memory interrupt
- Eight General Purpose Input (GPI) and eight General Purpose Output (GPO) pins for host assignment
- DTE interface: two alternate ports
  - Selectable microprocessor bus (6500 or 8085)
  - ITU-T V.24 (EIA/TIA-232-E compatible) interface
- TTL and CMOS compatible
- 3.3V/5V operation
- Power consumption
  - Operating Mode: 200 mW (Basic), 275 mW (-V option). 300 mW (-VS option)
  - Sleep Mode: 1 ma (Basic. -V option and -VS option)
- Packaging
  - 128-pin TQFP (thin quad flat pack)

FM209 (IC4) Hardware Interface Signals

Pin Signals – 128-Pin TQFP

Pin No.	Signal Name	I/O Type	Pin Description
1	SR4IN/RESERVED	MI	Modem Interconnect
2	SR3OUT/RESERVED	MI	Modem Interconnect
3	EYESYNC	OA	Eye Pattern Circuit
4	EYECLK	OA	Eye Pattern Circuit
5	RXD	OA	DTE serial interface
6	SR1IO	MI	Modem Interconnect
7	NC	—	No Connection
8	EYEXY	OA	Eye Pattern Circuit
9	SR4OUT	MI	Modem Interconnect
10	VDD1	PWR	3.3V Digital Supply for DSP
11	RLSD#	OB	DTE Serial Interface
12	DCLK	OB	DTE Serial Interface
13	EN85#	IA	Host Parallel Interface
14	GPI0	IA	Host Parallel Interface
15	RTS#	IA	DTE Serial Interface
16	DGND1	GND	DSP Digital Ground
17	TXD	IA	DTE Serial Interface
18	SA1CLK	MI	Modem Interconnect
19	RS4	IB	Host Parallel Interface
20	RS3	IB	Host Parallel Interface
21	RS2	IB	Host Parallel Interface
22	RS1	IB	Host Parallel Interface
23	RS0	IB	Host Parallel Interface
24	YCLK	I	Modem Interconnect
25	IACLK	MI	Modem Interconnect
26	IA1CLK	MI	Modem Interconnect
27	CTRLSIN_S/NC	MI	Modem Interconnect
28	RESERVED/NC	MI	Modem Interconnect
29	SOUT_S/NC	MI	Modem Interconnect
30	SIN_S/NC	MI	Modem Interconnect
31	FSYNC_S/NC	MI	Modem Interconnect
32	IARESET_S#/NC	MI	Modem Interconnect
33	AGND1	GND	IA Analog Ground
34	LINEIN_S/NC	I	Line Interface
35	MICP_S/NC	I	Microphone Input
36	MICM_S/NC	I	Microphone Input
37	MICBIAS_S/NC	O	Microphone Bias Output
38	NC	—	No Connection
39	NC	—	No Connection
40	VREF_S/NC	MI	Modem Interconnect
41	VC_S/NC	MI	Modem Interconnect
42	VAA_S/NC	PWR	5V IA Analog power
43	LINEOUT_S/NC	O	Line Interface
44	NC	—	No Connection
45	AGND2	GND	IA Analog Ground
46	SPKRP_S/NC	O	Speaker Interface Output
47	SPKRM_S/NC	O	Speaker Interface Output
48	AVDD_S/NC	PWR	5V IA Digital power
49	RESERVED/NC	MI	Modem Interconnect
50	ICLK_S/NC	MI	Modem Interconnect
51	MCLK_P	MI	Modem Interconnect
52	CTRLSIN_P	MI	Modem Interconnect
53	RESERVED	MI	Modem Interconnect
54	SOUT_P	MI	Modem Interconnect
55	SIN_P	MI	Modem Interconnect
56	FSYNC_P	MI	Modem Interconnect
57	IARESET_P#	MI	Modem Interconnect
58	AGND3	GND	IA Analog Ground
59	NC	—	No Connection
60	LINEIN_P	I	Line Interface
61	MICP_P	I	Microphone Input
62	MICM_P	I	Microphone Input
63	MICBIAS_P	O	Microphone Bias Output
64	NC	—	No Connection
65	NC	NC	No Connection
66	VREF_P	MI	Modem Interconnect
67	VC_P	MI	Modem Interconnect
68	VAA_P	PWR	5V Analog Supply for IA
69	LINEOUT_P	O	Line Interface
70	AGND4	GND	IA Analog Ground
71	SPKRP_P	O	Speaker Interface Output

FM209 (IC4) Hardware Interface Signals

Pin Signals – 128-Pin TQFP

Pin No.	Signal Name	I/O Type	Pin Description
72	SPKRM_P	O	Speaker Interface Output
73	AVDD_P	PWR	5V Digital power for IA
74	NC	—	No Connection
75	ICLK_P	MI	Modem Interconnect
76	MCLK_S/NC	MI	Modem Interconnect
77	VDD2	PWR	3.3V Digital Supply for DSP
78	D7	IB/OC	Host Parallel Interface
79	D6	IB/OC	Host Parallel Interface
80	D5	IB/OC	Host Parallel Interface
81	D4	IB/OC	Host Parallel Interface
82	D3	IB/OC	Host Parallel Interface
83	D2	IB/OC	Host Parallel Interface
84	DGND2	GND	DSP Digital Ground
85	VDD3	PWR	3.3V Digital Supply for DSP
86	D1	IB/OC	Host Parallel Interface
87	DGND3	GND	DSP Digital Ground
88	D0	IB/OC	Host Parallel Interface
89	CSBR#	IB	Host Parallel Interface
90	WRITE#	IB	Host Parallel Interface
91	CS#	IB	Host Parallel Interface
92	READ#	IB	Host Parallel Interface
93	GPI2	IA	General purpose input
94	GPI3	IA	General purpose input
95	GPI4	IA	General purpose input
96	GPI5	IA	General purpose input
97	GPI6	IA	General purpose input
98	GPI7	IA	General purpose input
99	GPO7	OC	General purpose output
100	VDD4	PWR	3.3V DSP Digital Power
101	GPO6	OC	General purpose output
102	GPO5	OC	General purpose output
103	RESERVED	MI	Modem Interconnect
104	GPO4	OC	General purpose output
105	GPO3	OC	General purpose output
106	DGND4	GND	DSP Digital Ground
107	CTS#	OB	DTE Serial Interface
108	IRQ1#	OB	Interrupt request
109	GPO2	OC	General purpose output
110	GPO1	OC	General purpose output
111	GPO0	OC	GPO0 (IA reset)
112	VDD5	PWR	3.3V DSP Digital Power
113	VGG	PWR	5V DSP Digital
114	DGND5	GND	DSP Digital Ground
115	RESET#	IB	External reset
116	XTALI	I	Crystal in
117	XTALO	O	Crystal out
118	RESERVED	MI	Modem Interconnect
119	XCLK	OB	X clock output
120	GPI1	IA	General purpose input
121	IRQ2#	OA	Interrupt request
122	SR3IN	MI	Modem Interconnect
123	RESERVED	MI	Modem Interconnect
124	RESERVED	MI	Modem Interconnect
125	DGND6	GND	DSP Digital Ground
126	DVAA	PWR	3.3V DSP analog power
127	AGND5	GND	DSP Analog Ground
128	RESERVED	MI	Modem Interconnect

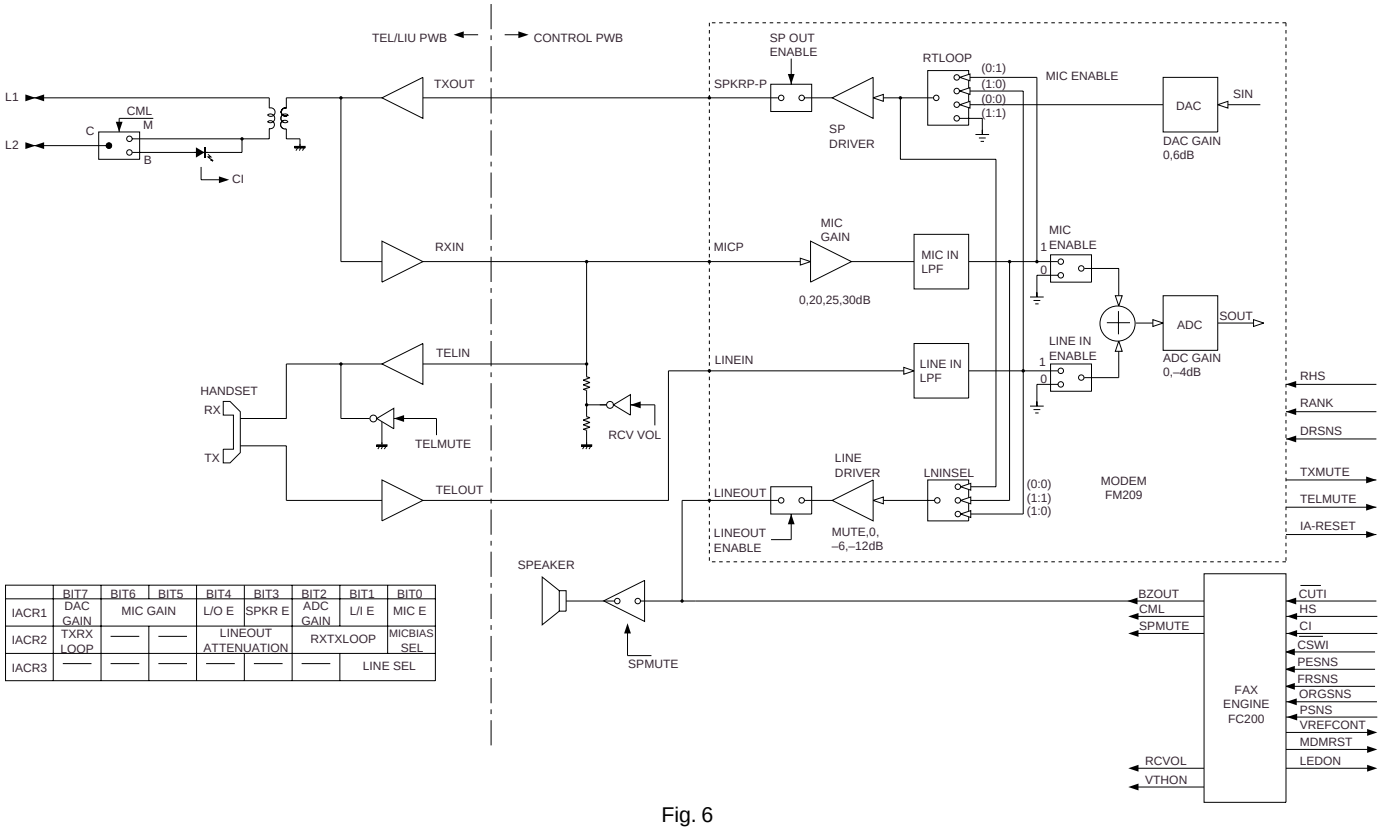
Notes:
I/O types: MI = Modem interconnect.
IA, IB, = digital input
OA, OB, OC = digital output
I = analog input
O = analog output

_P Signals: Primary IA
_S Signals: Secondary IA
Reserved = No external connection allowed.

[3] Circuit description of TEL/LIU PWB

(1) TEL/LIU block operational description

1) Block diagram



	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IACR1	DAC GAIN	MIC GAIN		L/O E	SPKR E	ADC GAIN	L/I E	MIC E
IACR2	TXRX LOOP	——	——	LINEOUT ATTENUATION		RXTXLOOP		MICBIAS SEL
IACR3	——	——	——	——	——	——	LINE SEL	

Fig. 6

2) Circuit description

The TEL/LIU PWB is composed of the following 7 blocks.

1. Speech circuit section
2. Dial transmission section
3. Speaker amplifier section
4. Ringer circuit section
5. Externally connected TEL OFF HOOK detection circuit
6. CI detection circuit
7. Signal/DTMF transmission level

3) Block description

1. Speech circuit section

- The receiver volume is an electronic volume type, this model is switched in 2 steps.

2. Dial transmission section

- D.P. transmission: The CML relay is turned on and off for control in the DP calling system. (Refer to the attached sheet.)
- DTMF transmission: It is formed in the modem, and is output.

3. Speaker amplifier section

- Ringer volume : It is controlled by the combination of the attenuator value of the LINE DRIVER in the modem and the ringer sending level sent from the modem.
- Speaker volume: It is controlled by the attenuator value of the LINE DRIVER in the modem.

4. Ringer circuit section

- The ringer sound is formed in the tone of modem when CI signal is detected. The amplifier circuit drives the speaker of the main body.

5. Externally connected TEL OFF HOOK detection circuit section

- The circuit current detection is turned on together with OFF HOOK of main body or OFF HOOK of externally connected TEL. ON of CML OFF ($\overline{HS}$=L) is judged as OFF HOOK of externally connected TEL.

6. CI detection circuit

- CI is detected by the photocoupler which is integrated in series in the primary side TEL circuit well proven in the existing unit.

7. Signal/DTMF transmission level

- Signal transmission level setting: ATT -10 dB Circuit output: -12 dBm.
- DTMF transmission level setting: HF -3.5 dBm LF -5.0 dBm Thus, set the level.

4) Signal selection

The following signals are used to control the transmission line of TEL/FAX signal. For details, refer to the signal selector matrix table.

[Control signals from output port]

Signal Name	Description
CML (The circuit is located in the TEL/LIU PWB.)	Line connecting relay and DP generating relay H: Line make L: Line break
SP MUTE (The circuit is located in the TEL/LIU PWB.)	Speaker tone mute control signal H: Muting (Power down mode) L: Muting cancel (Normal operation)
TEL MUTE	Handset reception mute control signal H: Muting L: Muting cancel
RCVOL (The circuit is located in the control PWB.)	Handset receiver volume control signal Volume: High / Low / DTMF sending and LOW RCVOL: L / H / H Note: The DTMF sending listed above is DTMF signal sending in the handset OFF-HOOK mode.

VOLUME SETTING		LINEOUT A (HIGH)	LINEOUT A (LOW)	RCVOL
Receiver volume setting	Low			1
	High			0
DTMF Transmission volume setting (Receiver)	Fixed			1
Key buzzer volume setting	Fixed			
Speaker volume setting	Low	1	1	
	Middle	1	0	
	High	0	1	
Ringer volume setting	Low	1	1	
	Middle	1	0	
	High	0	1	
DTMF speaker volume setting	Low	1	1	
	Middle	1	0	
	High	0	1	

[Signals for status recognition according to input signals]

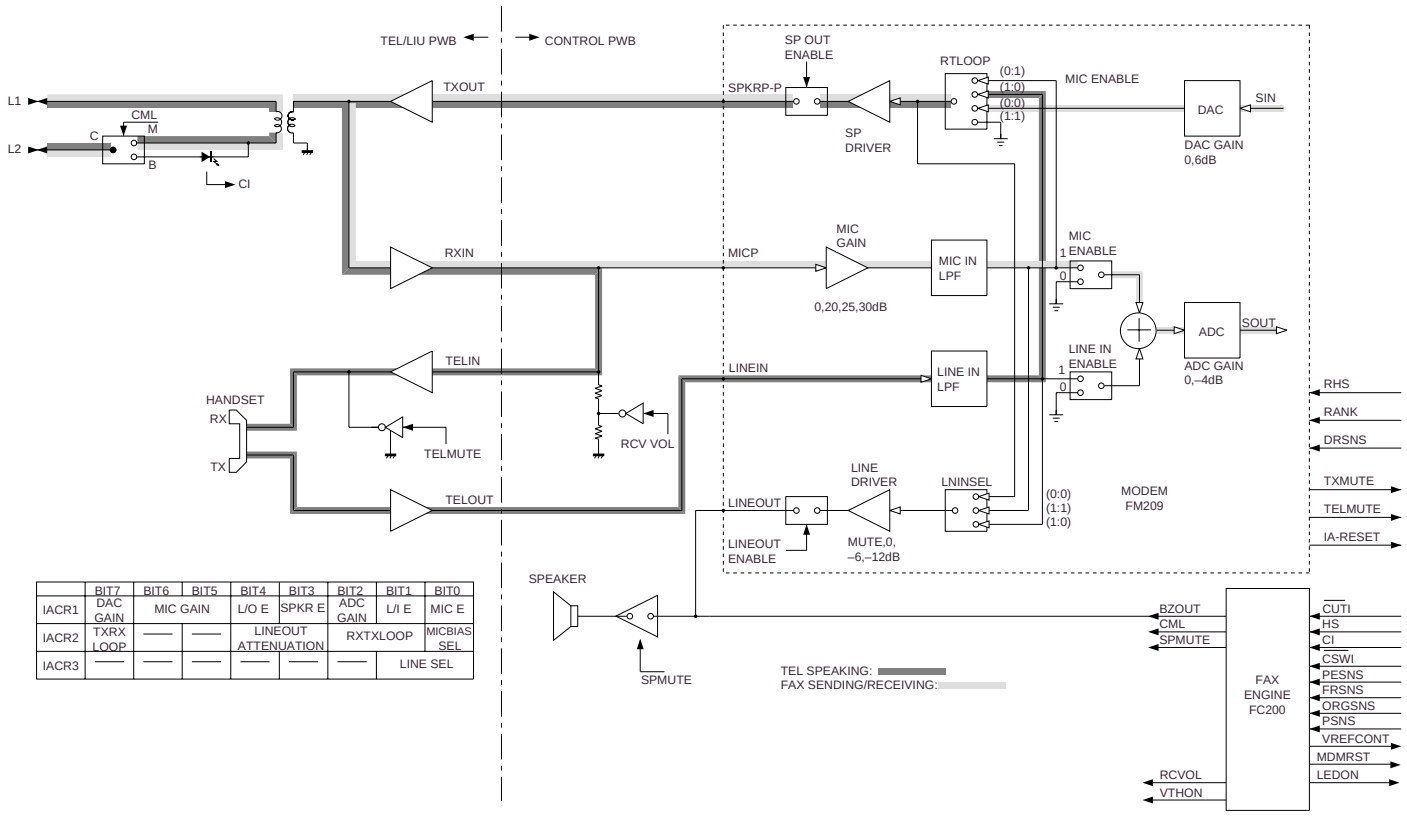
Signal Name	Function
$\overline{\text{RHS}}$	H: The handset is in the on-hook state. L: The handset is in the off-hook state.
CI	Incoming call (CI) detection signal

[Other signals]

Signal Name	Function
TEL IN	Receiving signal from line or modem
TEL OUT	Transfer signal to line
SPOUT	Speaker output signal
TXOUT	Transmission (DTMF) analog signal output from modem
RXIN	Reception (DTMF, others) analog signal input into modem

NO	Signal Name (CNLIUA)	NO	Signal Name (CNLIUA)
1	TELOUT	7	RXIN
2	TELIN	8	TXOUT
3	TELMUTE	9	CML
4	CI	10	+5V
5	HS	11	DG
6	$\overline{\text{RHS}}$	12	+24V

(Example: TEL speaking)



	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IACR1	DAC GAIN	MIC GAIN		L/O E	SPKR E	ADC GAIN	L/I E	MIC E
IACR2	TXRX LOOP	——	——	LINEOUT ATTENUATION		RXTXLOOP		MICBIAS SEL
IACR3	——	——	——	——	——	——	LINE SEL	

Fig. 7

[4] Circuit description of power supply PWB

1. Block diagram

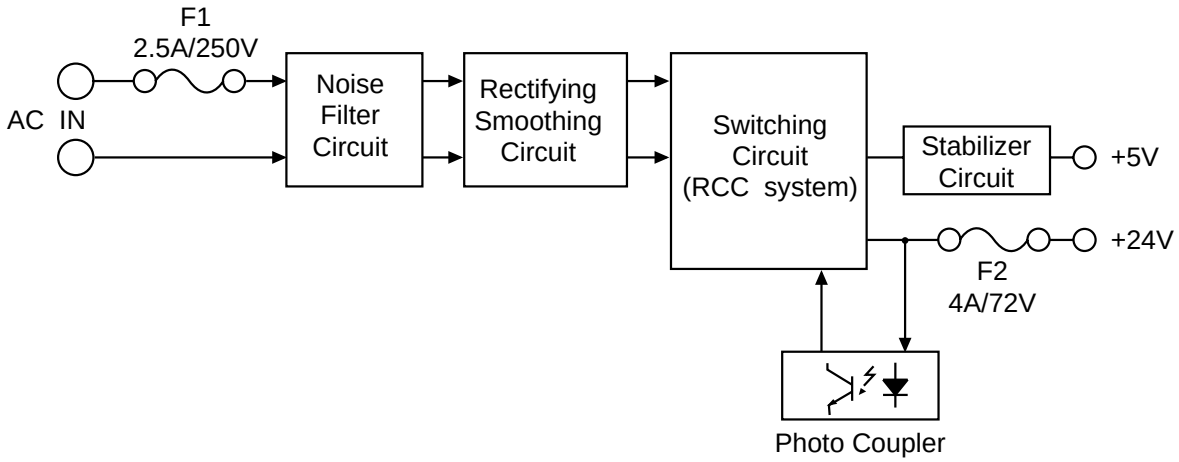


Fig. 8

2-1. Noise filter circuit

The input noise filter section is composed of L and C, which reduces normal mode noise from the AC line and common mode noise to the AC line.

2-2. Rectifying/smoothing circuit

The AC input voltage is rectified by diode D1, 2, 3, 4 and smoothed by capacitor C5 to supply DC voltage to the switching circuit section.

Power thermistor TH1 suppresses inrush current at power switch-on.

2-3. Switching circuit

This circuit employs the self excited ringing choke convertor (RCC) system. In this system, the DC voltage supplied from the rectifying/smoothing section is converted into high frequency pulses by ON/OFF repetition of MOS FET Q1.

Energy is charged in the primary winding of T1 during ON period of Q1, and discharged to the secondary winding during OFF period.

The output voltage is controlled by adjusting ON period of Q1 which changes charge time of C9 through operation of photo-coupler PC1 from +24V output.

The overcurrent protection is performed by bringing Q1 to OFF state through detection of voltage increase in the auxiliary winding of T1 by R5 and R7.

2-4. +5V circuit

Each DC voltage supplied by rectifying the output of transformer T1 with diode D9 is stabilized.

[5] Circuit description of CIS unit

1. CIS (Contact Image Sensor)

Cis is an image sensor which puts the original paper in close contact with the full-size sensor for scanning, being a monochromatic type with the pixel number of 1,728 dots and the main scanning density of 8 dots/mm.

It is composed of sensor, rod lens, LED light source, light-conductive plate, control circuit and so on, and the reading line and focus are previously adjusted as the unit.
Due to the full-size sensor, the focus distance is so short that the set is changed from the light weight type to the compact type.

2. Waveforms

The following clock is supplied from FC200 of the control board, and VO is output.

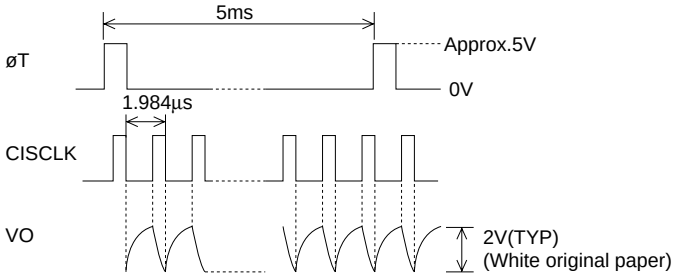


Fig. 9